computer system. Examples of the computer readable recording medium include read-only memory (ROM), random-access memory (RAM), compact disc (CD)-ROM, digital versatile disc (DVD), magnetic tape, floppy disk, and optical data storage device, not being limited thereto. The transmission medium can include carrier waves transmitted through the Internet or various types of communication channel. The computer readable recording medium can also be distributed over network coupled computer systems so that the computer readable code is stored and executed in a distributed fashion.

[0087] At least one of the components, elements, modules or units represented by a block as illustrated in FIG. **2** (e.g., address extractor **170**, first core **181**, second cores **183**, etc.) may be embodied as various numbers of hardware, software and/or firmware structures that execute respective functions described above, according to an exemplary embodiment. For example, at least one of these components, elements, modules or units may use a direct circuit structure, such as a memory, a processor, a logic circuit, a look-up table, etc. that may execute the respective functions through controls of one or more microprocessors or other control apparatuses. Also, at least one of these components, elements, modules or units may be specifically embodied by a module, a program, or a part of code, which contains one or more executable instructions for performing specified logic functions, and executed by one or more microprocessors or other control apparatuses. Also, at least one of these components, elements, modules or units may further include or may be implemented by a processor such as a central processing unit (CPU) that performs the respective functions, a microprocessor, or the like. Two or more of these components, elements, modules or units may be combined into one single component, element, module or unit which performs all operations or functions of the combined two or more components, elements, modules or units. Also, at least part of functions of at least one of these components, elements, modules or units may be performed by another of these components, elements, modules or units. Further, although a bus is not illustrated in the above block diagrams, communication between the components, elements, modules or units may be performed through the bus. Functional aspects of the above exemplary embodiments may be implemented in algorithms that execute on one or more processors. Furthermore, the components, elements, modules or units represented by a block or processing steps may employ any number of related art techniques for electronics configuration, signal processing and/or control, data processing and the like.

[0088] While exemplary embodiments have been particularly shown and described, it will be understood by those of ordinary skill in the art that various changes in forms and details may be made therein without departing from the spirit and scope of the inventive concept as defined by the following claims.

What is claimed is:

1. A data storage device comprising:

a non-volatile memory device; and

a controller configured to receive a command from a host and to control an operation of the non-volatile memory device based on the command, the controller comprising a processor configured to receive and process the command and an address extractor configured to extract address information from the command and to output the address information to the processor before the processor processes the command.

2. The data storage device of claim **1**, wherein the processor comprises:

a first core configured to generate a sub-command based on the command; and

a plurality of second cores configured to receive the sub-command output from the first core.

3. The data storage device of claim **2**, wherein the sub-command corresponds to commands for controlling peripheral devices comprised in the data storage device to perform one of a read operation and a write operation of the non-volatile memory device.

4. The data storage device of claim **2**, wherein the sub-command corresponds to one among a read operation, a write operation, and a trimming operation on peripheral devices comprised in the data storage device.

5. The data storage device of claim **2**, wherein the address information comprises logical address information corresponding to peripheral devices comprised in the data storage device.

6. The data storage device of claim **5**, wherein the logical address information comprises a namespace, a volume, a logical block address, and a length.

7. The data storage device of claim **2**, wherein the first core is configured to determine the command at a first time point and the address extractor is configured to output the address information to the plurality of second cores at the first time point.

8. The data storage device of claim **7**, wherein the plurality of second cores are configured to perform an operation of preparing to control peripheral devices comprised in the data storage device at the first time point based on the address information.

9. The data storage device of claim **8**, wherein the plurality of second cores are configured to determine, at the first time point, whether internal management data corresponding to the address information has been loaded to the controller; and load, in response to the determining indicating the internal management data has not been loaded, the internal management data corresponding to the address information from the non-volatile memory device at a second time point after the first time point.

10. The data storage device of claim **9**, wherein the sub-command comprise a command corresponding to an operation of loading the internal management data corresponding to the address information and a command corresponding to an operation of programming the non-volatile memory device based on the internal management data.

11. The data storage device of claim **10**, wherein the internal management data comprises map information corresponding to the address information among information corresponding to a logical address and a physical address which are comprised in a mapping table of the non-volatile memory device.

12. The data storage device of claim **2**, wherein each of the plurality of second cores is configured to determine whether to process the received sub-command based on the address information.

13. The data storage device of claim **12**, wherein the address information indicates a selected second core of the plurality of second cores, and only the selected second core processes the received sub-command.